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ENHANCING ENERGY EFFICIENCY OF SRAM THROUGH OPTIMIZATION OF SRAM ARRAY STRUCTURES

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ABSTRACT

Reliability is a major concern in the microprocessor industry. SRAM plays a significant role in energy consumption due to increases in computing power. In order to get high efficiency in the SRAM, the array structure has to be modified. In traditional practices where SRAM array enclose more number of rows than columns. Previously proposed techniques improve the efficiency by 10% for 8kbit and 40% for 64kbit for same SRAM bit density and same supply voltage. The proposed techniques such as deep sub micron technology are implemented for getting better reliability. Many proposed design concern only on the low power dissipation but generally degrade response time. The power consumption of the system on chip devices having SRAMs increase largely with technology scaling because at low scale, Gate leakage current, sub threshold current, tunnelling plays a significant role in the SRAM operation. This work reveals that better SRAM energy efficiencies can be achieved with a wider SRAM array structure with fewer rows than columns particularly at low supply voltage. In this proposed 10T cell shows better performance with reduced power consumption and different Temperature as against conventional 8T SRAM.

KEYWORDS: Low Scale, Gate Leakage Current, Sub Threshold Current

1. INTRODUCTION

Many of todays advanced CMOS device are being applied to low power applications like battery powered computers,telecommunication equipment and aerospace application.designers of these CMOS system need fast and acurate estimation of energy consumption for their designs.the most popular way of obtaining low energy consumption is to lower supply voltage to below or around the threshhold voltage[2]. Designing of SRAM in this operation region has been observed to be more challenging due to additional design constraints Compared to generic digital logic, and so, various circuit techniques have been published with successful hardware measurements [2]-[3]. Decoupled SRAM cells have been popularly deployed for improving cell stability [3]. Write margin issues have been tackled through several techniques using positively or negatively boosted voltage, strengthening the write access transistors utilizing channel length modulation, and Supply voltage can be driven by 10T[4]–[6].

In their work, the optimum SRAM array structures for minimized energy consumption were found to be non square and had more rows than columns, while the optimum array structures for minimizing the memory access time were squarer than those for the minimum energy consumption. However, this work only focused on the high-performance region where the static energy from the leakage current is insignificant compared to the dynamic energy. At ultralow supply voltage, the static energy becomes comparable to the dynamic energy [4], which requires the optimal SRAM array structure to be revisited.

In this brief, we analyze SRAM array structures for energy efficiency enhancement for ultralow-power systems. Commercial 65-nm low-power CMOS process technology is used for simulation. In Section II, we explain normal array structures. In Section III, we explain the dual Vth schemes and its effects on SRAM and ten transistors (10T) SRAM sub array under consideration and SRAM energy modelling. In Section IV, we analytically derive optimal SRAM array structures and analyze the effects of SRAM array structural change on energy consumption. Finally, Section V summarizes and concludes this work.

2. NORMAL ARRAY STRUCTURE

An SRAM cell must be designed such that it provides a non-destructive read and write operation. These requirements on SRAM cell transistor sizing. In this paper we implemented a novel SRAM cell for low-power applications. An SRAM cell is designed to provide non-destructive read access, write capability and data storage (or data retention) for as long as cell is powered. We will discuss design and analysis of two different SRAM cells: a six-transistor (6T), (8T) and (10T). We will compare them with respect to power. In general, the cell design must strike a balance between cell area, robustness, speed, leakage and yield. Power reduction is one of the most important design objectives.

2.1. SRAM Array

Larger SRAM arrays can be constructed from smaller ones. For this example, we want to build an 8x4 SRAM array. The external interface of the array should be as if it were a single SRAM structure, as shown at right. To see where different parts of the data are stored for each design, values are given inside the RAM structures for each address location (address at right in decimal, binary data at right in the colour boxes). All designs of the 8x4 SRAM hold the same 4-bit data at the same 3-bit address locations [7]. This can be shown in the figure 1.

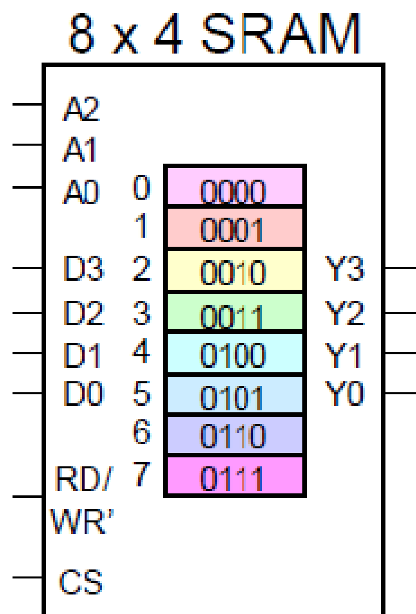

Figure 1: 8:4 SRAM

2.1.1 Building Wider SRAMS

We can use multiple SRAMs to make a wider device. The data inputs/outputs are split between the SRAM components. The address, chip select, and RD/WR' signals are the same for all devices. Each device contains a subset of the bit positions for all of the memory's words. We can use multiple SRAMs to make a device with more row locations.

The input data lines, RD/WR' signal this can be shown in the figure 2, and lower address bits are the same for all chips. The upper address bits and the CS input generate the individual chip selects.

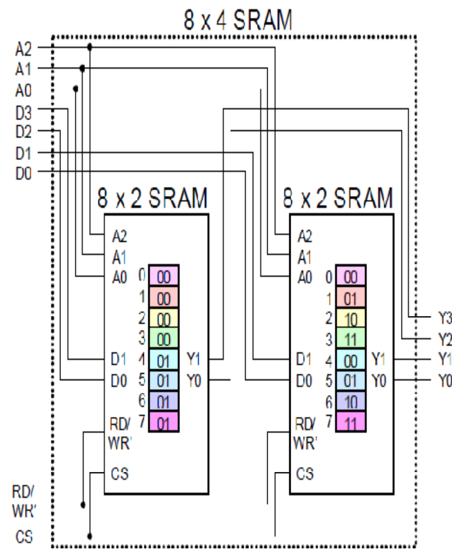

Figure 2: Wider SRAM Cell

2.2. SRAM Array with 6T Cell

The mainstream six-transistor (6T) CMOS SRAM cell is shown in Figure 3, four transistors (Q1−Q4) comprise cross-coupled CMOS inverters and two NMOS transistors Q5 and Q6 provide read and write access to the cell. A 6T SRAM cell is the most popular SRAM cell due to its low power and low-voltage operation.

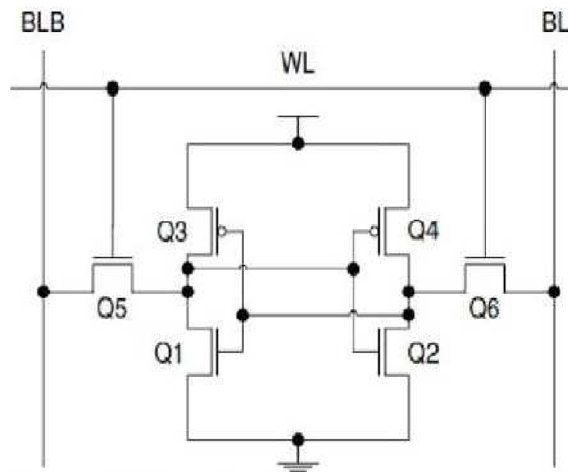

Figure 3: 6T CMOS SRAM Cell

3. 8T AND 10T SRAM ARRAY STRUCTURE AND ENERGY ESTIMATION

In this section, we will discuss the effect of dual Vth scheme on SRAM, the structure of 8T and 10T SRAM, and the analytical modelling of different design parameters that play a key role in determining the total energy of SRAM. We selected 10T SRAM for our energy analysis, and the following section explains the reason behind this selection.

3.1. Proposed Dual Vth Scheme Effect ON SRAM

For the 6T SRAM, the cell stability and the write ability may sporadically experience data-flipping (i.e., a bit cell changes its state from '0' to '1' or *vice versa* after being read) or write failure (i.e., the data to be written into

a bit cell fails to overwrite its previously stored value). To cope with these problems, several new SRAM cells equipped with some supportive peripheral circuits have been proposed like the single-ended sensing cells [4]–[8] and differential sensing cells [9], [10]. In general, a single-ended sensing cell is not as robust as the differential one, and hence, it often requires some extra compensation scheme to maintain the reliability as proposed in [7].

Moreover, it is not easy if not impossible for a single-ended sensing cell to support column multiplexing (also known as *bit-interleaving*) in which an IO is shared among several cell columns. In the differential cells, the stability and write ability of the cell have been improved by using two cross-coupled Schmitt-trigger inverters to form the storage cell. There is a minor problem with this type of *ST cell* – it still suffers from the *read disturbance problem*, which refers to the phenomenon that a storage node with data '0' will experience a *transient voltage glitch* when it is being read. This voltage glitch may sometimes cause the cell to flip unexpectedly.

In our work, we have used dual Vth scheme in 10T SRAM cell. The working of this cell is the same as the standard Vth 10T SRAM cell except for the access transistors (PGL and PGR), which are used here, have low Vth and the pull-down transistors (PDL2 and PDR2) have high Vth. As explained earlier, due to the low Vth of the access transistors, the access speed of the transistors increases considerably. This helps in faster access of the data stored in the SRAM cell. Also due to the high Vth pull-down transistors, the leakage of the circuit through theses transistors decreases. Hence, the performance of the cell increases as compared to the dual Vth 8T SRAM cell on an area-power trade-off.

3.2. 8T SRAM Cell

A 8T SRAM cell consisting of 6T and 2 n MOS transistors, it also consists of 2pull-up pMOS transistors and 2pull-down nMOS transistors is shown in the following figures (Elmasry, 2000).The single-port SRAM consists of one set of address line and data storage. Hence, the SRAM may do the read-operation or write-operation at the same time, so it is called as "1WR". However, from the Figure 5 two write-read (2WR) type of 8T-SRAM which has same structure with the standard single-port 8T SRAM. But it contains two set of data storage and address line. By this definition, we can called as dual-port memory cell. Each address line and data storage can complete the write and read operation separately. Figure 6 is also a Data Path storage cell, which also has 2 sets of address line and data storage, how where in this one can do write and the other can do the read operation (1W1R). In these 8T-SRAM contain 2 types, the 2WR type can also operate as a 1W1R, but the 1W1R type cannot operate as 2WR cell.

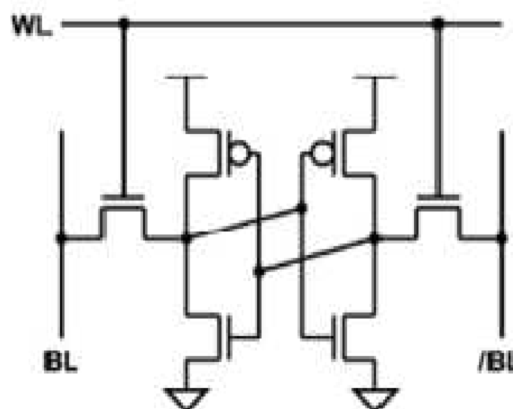

Figure 4: 6T Cell

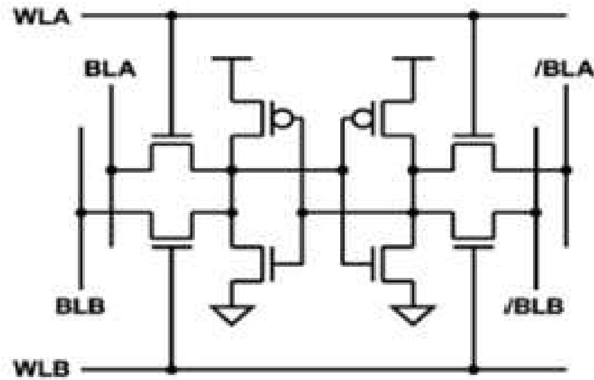

Figure 5: 8T Cell (1 Write)

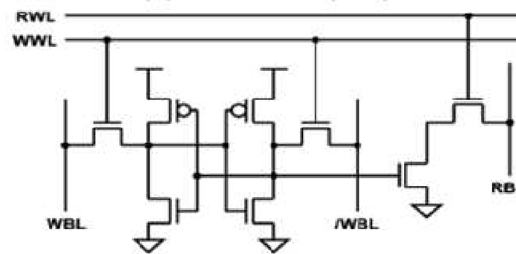

Figure 6: 8T Cell (1 Read 1 Write)

As such, the 2 WR cell has more flexibility than 1W1R cell. In many SOC designs, 1WR SRAM is used to store the instructions. Hence, memory cell can be used to transfer registers and general purpose registers, where the memory contains 1 write port and 1 read port is needed. So, the structure showed in Figure 3 is used in the system proposed by Kai-ji *et al.* [11] and Nii *et al.* (2009). As there are three kinds of Data Path SRAM, we handle the 8T SRAM and 10T SRAM with a single read port and 10T SRAM with differential read ports. Soft errors and Single Event Upsets (SEU) are common problem in memory circuits. This SEU can be occurred when a charged particle strikes a node and flips the state of the SRAM cell from 0 to 1 and as the same it causing a soft error also.

There are many solutions to increase the level of soft error protection of the SRAM cell. This Protection method is an effective method which uses capacitors in SRAM cells to absorb the excessive charge [12]. Although the SRAM provides a sufficient protection, they affect the cell performance also. Hence, do not needs to be refreshed those data. On the other hand, data that is stored in 1 transistor, 1 capacitor DRAM cell can get degraded over a period of time due to the leakation of charge. Therefore, for any high-speed operation, we can choose the SRAM memory as a choice.

The advantage of using 2 DP arrays is that once the data can be written into the memory cell, the data can be accessed from either the both port. For example, data that is written into the first array RAM-A in a first word line W1 can be accessed from either the left or right port of the array for a read operation. Hence not to disturb the unselected cells, in the each cycle 1 word line of the dual-port array is activated.

The 10T SRAM with a single read port is the best as a dual-port SRAM. Though the 8T SRAM has the least transistor count and it has high area efficient, the read output power becomes large and the cycle time increases due the read bit lines. The 10T SRAM can operate very fast. By using the power efficiency, the sense point is 50 mV, most cells use the bit line more than 50 mV, which leads to the power ahead. As a result, the 10T SRAM always consumes the lowest readout power.

3.3. Proposed 10T SRAM Cell

A 10T SRAM cell, Figure 2, as the name suggests, consists of 10 transistors. Out of these transistors, four are pull-up transistors (PUL1, PUL2, PUR1 and PUR2), four are pull down transistors (PDL1, PDL2, PDR1 and PDR2) and two are access transistors (PGL and PGR)[3]. The two pull-down transistors i.e. PDL1 and PDR1 are connected to VGND. This VGND signal is connected to ground during the read operation and VDD, otherwise. In 10T SRAM cell, the access transistors are connected to pseudo nodes (pQ and pQb i.e. nodes between two pull-up transistors) rather than the storage nodes (i.e. Q and Qb).

Due to this, the storage nodes are isolated from the BLs and therefore during the read operation, the read current does not flow through the storage nodes and hence maintain the read stability. In case of the write operation, the VGND is connected to VDD and one of the bit-lines get grounded. If the node Q is storing '1' and node Qb is storing '0'. When a high supply voltage is provided, the node Q is pulled down to '0' due to discharging through the access and the pull-up transistor i.e. PGL and PUL2.

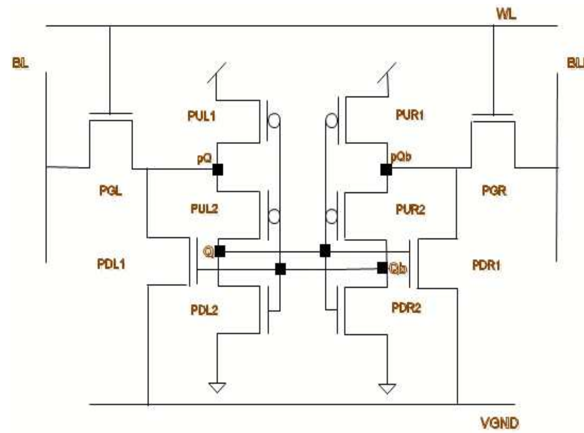

Figure 7: 10T SRAM Cell

In this paper we have proposed a 10T SRAM cell using dual- Vth scheme. Here, we use standard Vth pull-up transistors, low Vth access transistors and high Vth pull-down transistors. Due to the low Vth transistors, the gate voltage (Vg) required for activation of the access transistors is low and thus, the access speed for the data stored increases considerably. Also the high Vth Pull-down transistors decrease the leakage in the circuit.

4. SIMULATION WORK

In our work, we have used dual Vth scheme in 10T SRAM cell. The working of this cell is the same as the standard Vth 10T SRAM cell except for the access transistors (PGL and PGR), which are used here, have low Vth and the pull-down transistors (PDL2 and PDR2) have high Vth scheme. As explained earlier, due to the low Vth of the access transistors, the access speed of the transistors increases considerably. This helps in faster access of the data stored in the SRAM cell.

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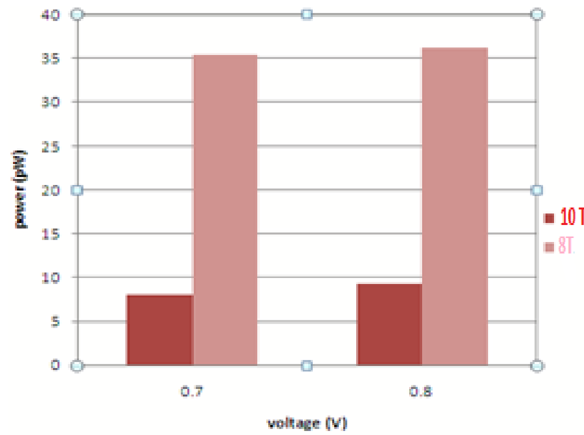


Figure 8: Comparison of Leakage Power of 8T and 10T

Figure 8 shows the static power dissipation of the dual-Vth 8T SRAM cell and the dual Vth 10T cell. As can be seen from the figure, the leakage power in dual-Vth 10T SRAM cell decreases by 74% and 77% as compared to the dual Vth 8T SRAM cell at VDD=0.8V and 0.7V respectively, at room temperature.

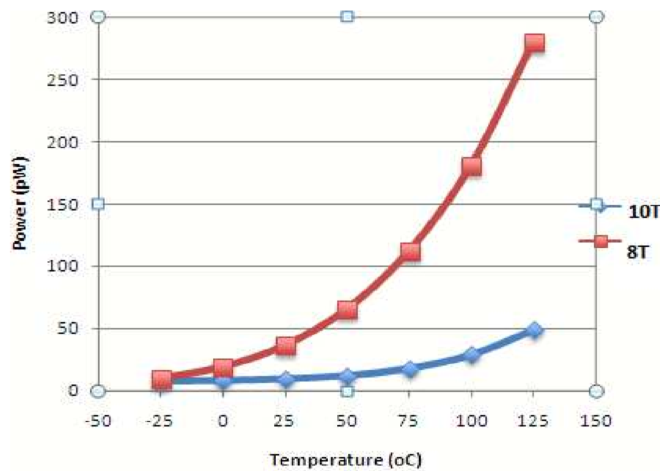
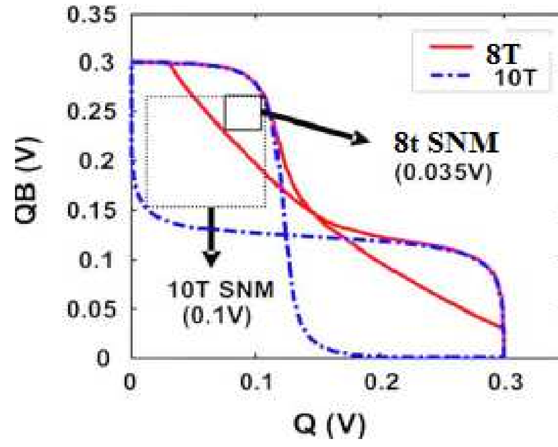


Figure 9: Effect of Temperature Variations on Conventional 8T and 10T SRAM Cell

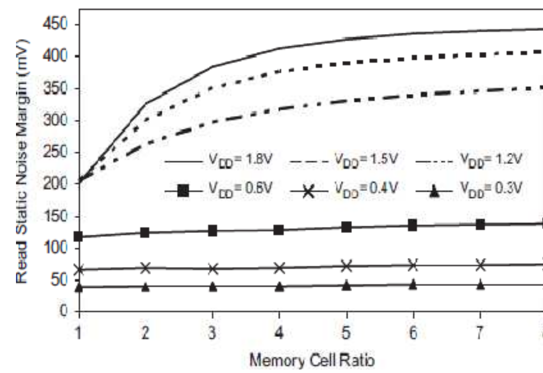
Figure 9 shows the temperature variation of the dual-Vth 8T and 10T SRAM cell over the temperature range –25 to 125 °C at 0.8V. In the dual Vth 10T SRAM cell, the leakage power decreases by 57%, 74%, 81% and 82 % at 0°C, 25°C, 50°C and 125°C, respectively as compared to dual-Vth 8T SRAM bit-cell. Apart from the reduction in the stand-by leakage, the cell has shown considerably good amount of SNM i.e. 0.42V at VDD=0.8V and 0.37V at VDD=0.7V. Thus, the only parameter where the cell compromise, is its area as it uses 10 transistors instead of 8T.

4.1. Results and Discussions

In the 8T SRAM, an access time is a period from a time at which an RWL rises to VDD/2.In the 10T SRAM, an access time is a higher one: a periods from a time at which a read word line (RWL) rises to VDD/2 to a time at which an output of the sense amplifier is charged up to VDD/2 to a time that an output of the sense amplifier is discharged down to VDD/2. In the 10T SRAM, an access time is a period from a time at which an RWL rises to VDD/2 to a time at which a differential voltage between an RBL it is expanded to 50 mV, 100 mV or 200 mV. In all the SRAMs, the worst cell with the worst threshold- voltage variation determines the delay. In particular, in the 10T-D SRAM, even if the sense point is set to 50 mV, most cells use the bit line more than 50Mv.



(a)



(b)

Figure 10: Statistical Analysis of 10T (a) SNM Ratio of 8T and Proposed 10T and (b) Read SNM of Different Voltage in 10T

Thus from the output of 10t we enhance the energy efficiency of SRAM array structure and SNM ratio of 10t can be simulated which is shown in the figure 10 (a) and (b).thus we conclude the comparison of different transistor shows that 10T can be used for better energy efficiency which is shown in the table 1.

Table 1: Comparison of Transistor

No of Transistor	Power	Area	Efficiency
4T	1.792mW	$4.1mm^2$	23.6%
6T	2.270mW	$5.9mm^2$	29.8%
8T	0.321mW	$6.2mm^2$	40%
10T	0.024µW	$2.2mm^2$	50%

5. CONCLUSIONS

In this paper, an analysis and simulation on P-P-N based 10T SRAM cell using dual-Vth scheme (at deep sub-micron technology) is presented. This work achieved stand-by leakage reduced by 74% and 77% as compared to dual-Vth 8T SRAM bit-cell at VDD=0.8V and VDD=0.7V, and energy efficiency increased by 50% and 20% respectively without losing cells performance at an area power-trade-off.

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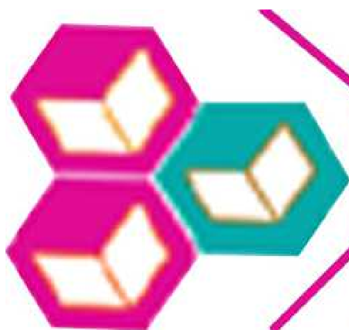

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